Specifications

DVB-S2 DUAL NIM

SP4336SVb

#1001, Sunil Technopia, Sangdaewon-dong,
Jungwon-gu, Seongnam City, Gyeonggi-do,
Korea, 462-120

Description: The open DVB-S2 standard for advanced modulation [8PSK modulation With LDPC/BCH Forward Error Correction], as well as legacy DVB and DSS specification

1. General Specifications of RF Tuner (STV6120).

1-1	Receiving Frequency Range	250~ 2150MHz
1-2	RF Input Impedance	75Ω
1-3	Channel Selection System	Built in PLL (I^2C Bus : Link IC)
1-4	RF input Connector	F Type (Female)
1-5	PLL Step Size	Depending on PLL Setting
1-6	Operating Voltage	LNB Power : (TYP) +3.3VL : 3.3V DC (± 5%) +3.3VT : 3.3V DC (± 5%) AGC Voltage : 0.5V ~ 2.5V DC
1-7	Current Consumption in Tuner Part	<table><tr><th></th><th>MIN</th><th>TYP</th><th>MAX</th></tr><tr><td>+3.3VL</td><td></td><td>44mA</td><td>59mA</td></tr><tr><td>+3.3VT</td><td></td><td>414mA</td><td>571mA</td></tr></table>
1-8	Temperature	Operating: 0℃ to 70℃ Storage: -40℃ to 125℃
1-9	Humidity	Operating: less than 85% Storage: less than 90%

2. Electrical Specifications of RF Tuner (STV6120)

Optimal Test Condition :

1. Supply Voltage : 3.3V ± 0.3V DC
2. Ambient Temperature: 25℃ ± 5 %
3. Ambient Humidity: 65% ±1 0%

No	Item	Specification				Condition
		Min	Typ	Max	Unit	
2-1	Input Level	-65		-25	dBm	
2-2	RF Input VSWR		2	3	dB	
2-3	Noise Figure		6	10	dB	
2-4	3'rd order Intermodulation Rejection Ratio	40	50		dB	Desired & Undesired input Level are -25dBm
2-5	Local Oscillation Signal leakage at RF Input Terminal			-70	dBm	950 ~ 2150 MHz
2-6	Gain Variation		4		dB	950 ~ 2150 MHz
2-7	Isolation		60		dB	
2-8	Phase Noise 10KHz Offset Freq 100KHz 1MHz		-87 -97 -110		dBc/Hz	

3. Programming

3.1 I2C Bus Protocol (STV6120)

The following call address has been allocated to the STV6120.

STV6120 I²C address

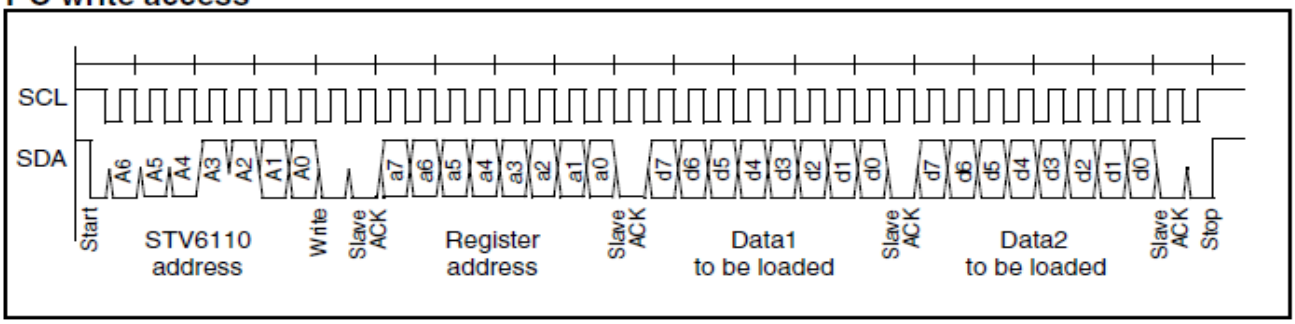
A6	A5	A4	A3	A2	A1	A0	RW
1	1	0	0	0	A1	A0	0: Write 1: Read

Addresses selected by pin AS

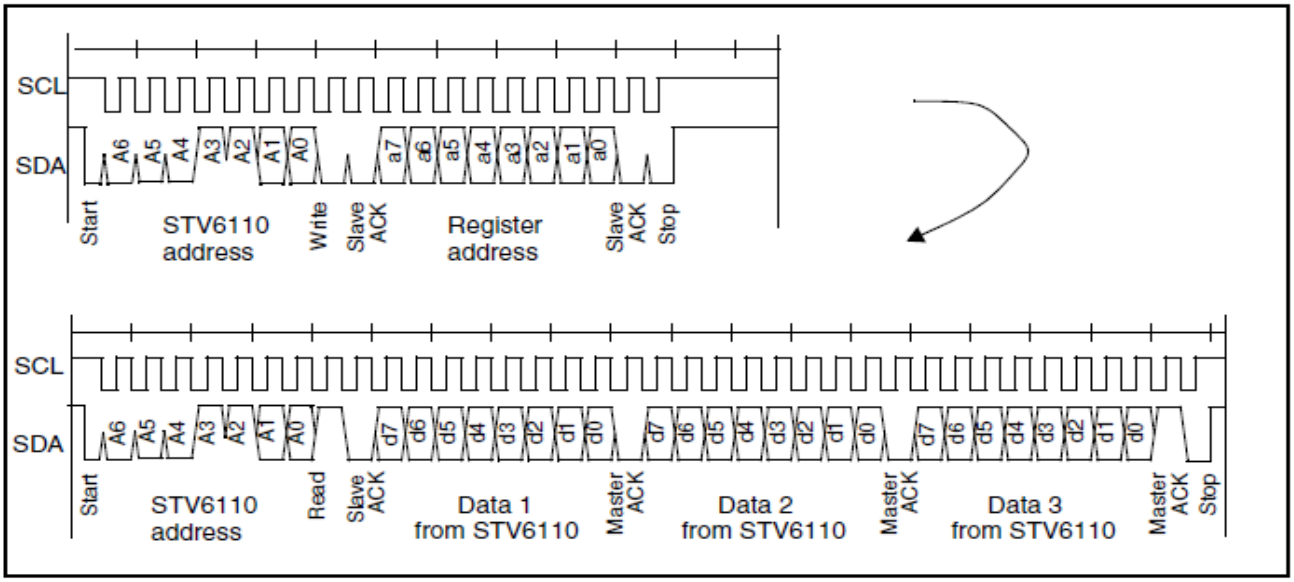
DC level on pin AS	A1	A0
GND_DIG	0	0
Open-circuit (not connected)	1	1

The current I2C address is fixed at 0xC0, that is, each A1,A0 bit is set to 0, 0

I²C write access



I²C read access



3.2 Register Map (STV6120)

Name	Addr	Reset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CTRL1	0x00	0x75	K4	K3	K2	K1	K0	Rdiv	Odiv	MCLKdiv
CTRL2	0x01	0x33	DCLOOPoff_1	SDoff_1	Syn_1	REFOUTsel_1	BBGain3_1	BBGain2_1	BBGain1_1	BBGain0_1
CTRL3	0x02	0xCE	N7_1	N6_1	N5_1	N4_1	N3_1	N2_1	N1_1	N0_1
CTRL4	0x03	0x54	**F6_1**	**F5_1**	**F4_1**	**F3_1**	**F2_1**	**F1_1**	**F0_1**	N8_1
CTRL5	0x04	0x55	F14_1	F13_1	F12_1	F11_1	F10_1	F9_1	F8_1	F7_1
CTRL6	0x05	0x0D	Reserved	**ICP2_1**	**ICP1_1**	**ICP0_1**	VCOIlow_1	F17_1	F16_1	F15_1
CTRL7	0x06	0x32	RCclkoff_1	Pdiv1_1	Pdiv0_1	CF4_1	CF3_1	CF2_1	CF1_1	CF0_1
CTRL8	0x07	0x44	TCAL1	TCAL0	CALtime_1	CFHF4_1	CFHF3_1	CFHF2_1	CFHF1_1	CFHF0_1
STAT1	0x08	0x0E	Reserved for test; set to 0				**Reserved**	CALVCOstrt_1	CALRCstrt_1	LOCK_1
CTRL9	0x09	0xF9	**Reserved**				RFsel1_2	RFsel0_2	RFsel1_1	RFsel0_1
CTRL10	0x0A	0x7F	**Reserved**		LNADon	LNACon	LNABon	LNAAon	PATHon_2	PATHon_1
CTRL11	0x0B	0x33	DCLOOPoff_2	SDoff_2	Syn_2	REFOUTsel_2	BBGain3_2	BBGain2_2	BBGain1_2	BBGain0_2
CTRL12	0x0C	0xCE	N7_2	N6_2	N5_2	N4_2	N3_2	N2_2	N1_2	N0_2
CTRL13	0x0D	0x54	**F6_2**	**F5_2**	**F4_2**	**F3_2**	**F2_2**	**F1_2**	**F0_2**	N8_2
CTRL14	0x0E	0x55	F14_2	F13_2	F12_2	F11_2	F10_2	F9_2	F8_2	F7_2
CTRL15	0x0F	0x0D	Reserved	**ICP2_2**	**ICP1_2**	**ICP0_2**	VCOIlow_2	F17_2	F16_2	F15_2
CTRL16	0x10	0x32	RCclkoff_2	Pdiv1_2	Pdiv0_2	CF4_2	CF3_2	CF2_2	CF1_2	CF0_2
CTRL17	0x11	0x44	Reserved		CALtime_2	CFHF4_2	CFHF3_2	CFHF2_2	CFHF1_2	CFHF0_2
STAT2	0x12	0x0E	Reserved		Reserved for test; set to 0		**Reserved**	CALVCOstrt_2	CALRCstrt_2	LOCK_2
CTRL18	0x13	0x00	Reserved for test; set to 0							
CTRL19	0x14	0x00	Reserved for test; set to 0							
CTRL20	0x15	0x4C	Reserved for test; set to 0x4C							
CTRL21	0x16	0x00	Reserved for test; set to 0							
CTRL22	0x17	0x00	Reserved for test; set to 0							
CTRL23	0x18	0x4C	Reserved for test; set to 0x4C							

3.3 Register Description (STV6120)

CTRL2 Circuit configuration and BB gain setting (path1)

7	6	5	4	3	2	1	0
DCLOOP off_1	SDoff_1	Syn_1	REFOUT sel_1	BBGAIN_1[3:0]			

Address: 0x01
Type: RW
Reset: 0x33
Description:

7 DCLOOPoff_1: selects the DC offset compensation loop (path 1):
0: compensation enabled (default) 1: compensation disabled

6 SDoff_1: This bit set the operating level (path1).

5 Syn_1: This bit set the operating level (path 1).

Operating modes path1

SYN_1	SDoff_1	PATHon_1	Synthesizer	Mixer + LPF + baseband gain	Mode
0	1	0	Off	Off	Power down path 1
1	0	1	On	On	Power on path 1

4 REFOUTsel_1: sets the DC voltage on pins IP_1, IN_1, QP_1, QN_1:
0: VCC / 2 1: 1.25 V (default)

3:0 BBGAIN_1[3:0]: sets the baseband amplifier gain (path 1)
When the amplifier is on the gain is increased as follows:
0x0: 0 dB 0x1: 2 dB 0x2: 4 dB 0x3: 6 dB (default) 0x4: 8 dB
0x5: 10 dB 0x6: 12 dB 0x7: 14 dB 0x8: 16 dB 0x9-0xF: not used.

CTRL7 Post divider ratio and low pass filter (path 1)

7	6	5	4	3	2	1	0
RCclkoff_1	PDIV_1[1:0]		CF_1[4:0]				

Address: 0x06
Type: RW
Reset: 0x32
Description:

4:0 CF_1[4:0]: sets the low pass filter cut off frequency

0x00: 5 MHz	0x01: 6 MHz	0x02: 7 MHz	0x03: 8 MHz
0x04: 9 MHz	0x05: 10 MHz	0x06: 11 MHz	0x07: 12 MHz
0x08: 13 MHz	0x09: 14 MHz	0x0A: 15 MHz	0x0B: 16 MHz
0x0C: 17MHz	0x0D: 18 MHz	0x0E: 19 MHz	0x0F: 20 MHz
0x10: 21MHz	0x11: 22 MHz	0x12: 23 MHz	0x13: 24 MHz
0x14: 25 MHz	0x15: 26 MHz	0x16: 27 MHz	0x17: 28 MHz
0x18: 29 MHz	0x19: 30 MHz	0x1A: 31 MHz	0x1B: 32 MHz
0x1C: 33 MHz	0x1D: 34MHz	0x1E: 35 MHz	0x1F: 36 MHz

CTRL9 RF input selection

7	6	5	4	3	2	1	0
Reserved				RFsel_2[1:0][		RFsel_1[1:0]	

Address: 0x09
Type: RW
Reset: 0xF9
Description:

7:4 Reserved: Not used

3:2 RFsel_2[1:0]: This bit sets the selected RF input for path 2
- 00: RFAin selected
- 01: RFBin selected
- 10: RFCin selected (default)
- 11: RFDin selected

1:0 RFsel_1[1:0]: This bit sets the selected RF input for path 2
- 00: RFAin selected
- 01: RFBin selected (default)
- 10: RFCin selected
- 11: RFDin selected

CTRL10 Operating mode

7	6	5	4	3	2	1	0
Reserved		LNADon	LNACon	LNABon	LNAAon	PATHon_2	PATHon_1

Address: 0x0A
Type: RW
Reset: 0x7F
Description: A test setup register

7:6 Reserved: not used

5 LNADon: set on the LNA of RFDin input
- 0: LNA off
- 1: LNA on

4 LNACon: set on the LNA of RFDin input
- 0: LNA off
- 1: LNA on

3 LNABon: set on the LNA of RFDin input
- 0: LNA off
- 1: LNA on

2 LNAAon: set on the LNA of RFDin input
- 0: LNA off
- 1: LNA on

1 PATHon_2: set on the path 2
- 0: PATH 2 off
- 1: PATH 2 on

0 PATHon_1: set on the path 1
- 0: PATH 1 off
- 1: PATH 1 on

CTRL11 Circuit configuration and BB gain setting (path 2)

7	6	5	4	3	2	1	0
DCLOOP off_2	SDoff_2	Syn_2	REFOUT sel_2	BBGAIN_2[3:0]			

Address: 0x0B
Type: RW
Reset: 0x33
Description:

7 DCLOOPoff_2: selects the DC offset compensation loop (path 2):
0: compensation enabled (default) 1: compensation disabled

6 SDoff_2: This bit set the operating level (path 2).

5 Syn_2: This bit set the operating level (path 2).

Operating modes path2

SYN_2	SDoff_2	PATHon_2	Synthesizer	Mixer + LPF + baseband gain	Mode
0	1	0	Off	Off	Power down path 2
1	0	1	On	On	Power on path 2

4 REFOUTsel_2: sets the DC voltage on pins IP_2, IN_2, QP_2, QN_2:
0: VCC / 2 1: 1.25 V (default)

3:0 BBGAIN_2[3:0]: sets the baseband amplifier gain (path 2)
When the amplifier is on the gain is increased as follows:

0x0: 0 dB 0x1: 2 dB 0x2: 4 dB 0x3: 6 dB (default) 0x4: 8 dB
0x5: 10 dB 0x6: 12 dB 0x7: 14 dB 0x8: 16 dB 0x9-0xF: not used.

CTRL16 Post divider ratio and low pass filter (path 2)

7	6	5	4	3	2	1	0
RCclkoff_2	PDIV_2[1:0]		CF_2[4:0]				

Address: 0x10
Type: RW
Reset: 0x32
Description:

4:0 CF_2[4:0]: sets the low pass filter cut off frequency

0x00: 5 MHz	0x01: 6 MHz	0x02: 7 MHz	0x03: 8 MHz
0x04: 9 MHz	0x05: 10 MHz	0x06: 11 MHz	0x07: 12 MHz
0x08: 13 MHz	0x09: 14 MHz	0x0A: 15 MHz	0x0B: 16 MHz
0x0C: 17MHz	0x0D: 18 MHz	0x0E: 19 MHz	0x0F: 20 MHz
0x10: 21MHz	0x11: 22 MHz	0x12: 23 MHz	0x13: 24 MHz
0x14: 25 MHz	0x15: 26 MHz	0x16: 27 MHz	0x17: 28 MHz
0x18: 29 MHz	0x19: 30 MHz	0x1A: 31 MHz	0x1B: 32 MHz
0x1C: 33 MHz	0x1D: 34MHz	0x1E: 35 MHz	0x1F: 36 MHz

4. General Specifications of The FEC.

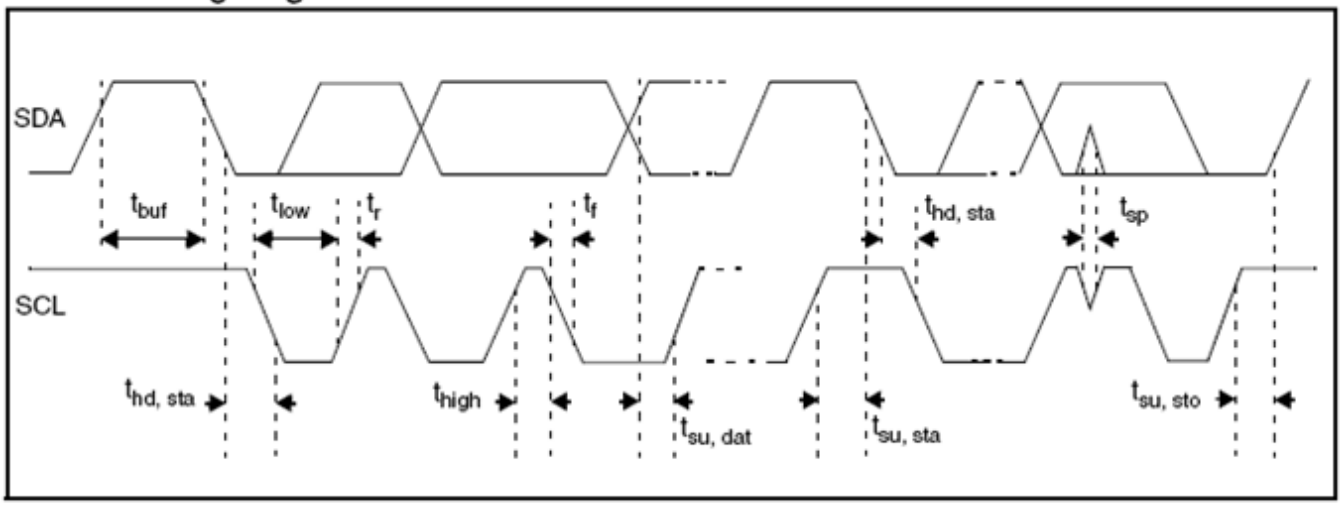
4-1	Temperature	- Operating: 0℃ to 70℃ - Storage: -40℃ to 125℃
4-2	Humidity	- Operating: less than 85% - Storage: less than 90%

<table>
<tr><th>No</th><th>Item</th><th>Specification</th></tr>
<tr><td>4-3</td><td>Symbol Rate</td><td>- QPSK/LDPC/BCH : 1MSps to 45MSps
- 8PSK/LDPC/BCH :1MSsps to 45MSps
- DVB QPSK : 1MSps to 62MSps</td></tr>
<tr><td>4-4</td><td>Code Rate</td><td>- DVB-S QPSK : 1/2, 2/3, 3/4, 5/6, 6/7, 7/8
- QPSK : 1/2, 3/5, 2/3, 3/4, 4/5, 5/6, 8/9, 9/10
- 8PSK : 3/5, 2/3, 3/4, 5/6, 8/9, 9/10</td></tr>
<tr><td>4-5</td><td colspan="2">Automatic acquisition: ±10 acquisition range</td></tr>
<tr><td>4-6</td><td colspan="2">I2C bus interface</td></tr>
<tr><td>4-7</td><td>Link IC</td><td>STV0900 (ST)</td></tr>
<tr><td>4-8</td><td>Data Output</td><td>Parallel or Serial Possible</td></tr>
<tr><td>4-9</td><td>Recommended Operating Voltage</td><td>
<table>
<tr><th>Symbol</th><th>Parameter</th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr>
<tr><td>3.3VD</td><td>Supply Voltage</td><td>3.0</td><td>3.3</td><td>3.6</td><td>V</td></tr>
<tr><td>1.0VD</td><td>Supply Voltage</td><td>0.95</td><td>1.05</td><td>1.15</td><td>V</td></tr>
</table>
</td></tr>
<tr><td>4-10</td><td>Current Consumption</td><td>1. DVB-S and DTV Legacy
- 3.3VD: 40 mA(Typ.)
- 1.0VD: 330 mA(Typ.) 2 Port DVB-S Active
2. DVB-S2
- 3.3VD: 40 mA(Typ.)
- 1.0VD: 650 mA(Typ.), 800 mA(Max) 2 Port DVB-S Active
3. Peak Current
- 1.0VD: 1.9 A(Max)</td></tr>
<tr><td>4-11</td><td>I2C Chip Address</td><td>AS0 pin: 0, Write- D0, Read- D1
AS0 pin: 1, Write- D2, Read- D3</td></tr>
</table>

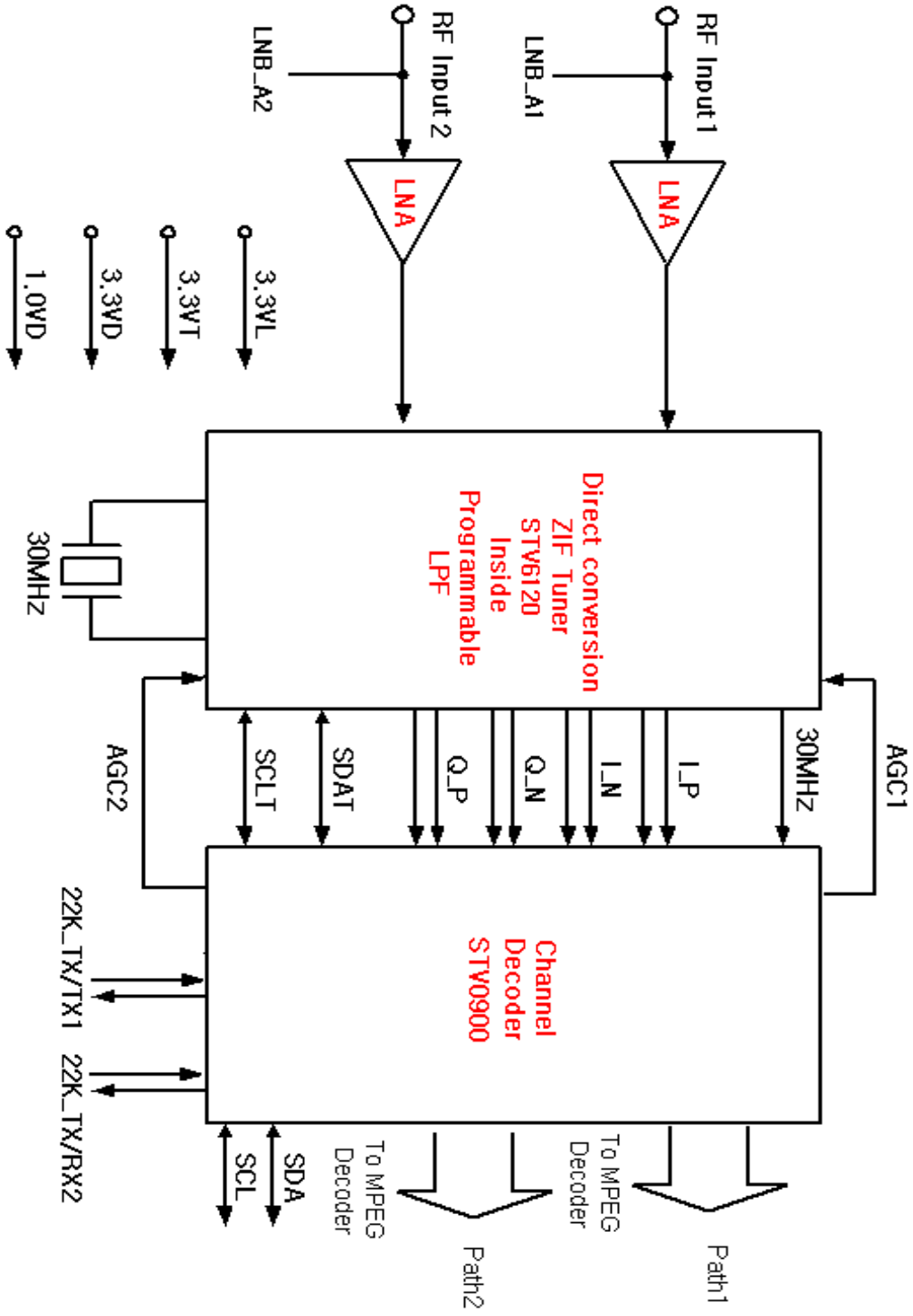
5. I2C Bus Specifications (STV0900)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
f_{scl}	SCL clock frequency	Normal mode	0		400	kHz
t_{buf}	Bus free time between a stop and start condition		1.3			µs
$t_{hd, sta}$	Hold time (repeated) start condition. After this period, the first clock pulse is generated.		0.6			µs
t_{low} t_{high}	Low period of the SCL clock High period of the SCL clock		1.3 0.6			µs µs
t_r	Rise time for SDA and SCL signals	Fast mode			300	ns
t_f	Fall time for SDA and SCL signals	Fast mode			300	ns
$t_{su, sta}$	Setup time for a repeated start condition		0.6			µs
$t_{su, sto}$	Setup time for stop condition		0.6			µs
$t_{su, dat}$	Data setup time		100			ns
t_{sp}	Pulse width of spikes to be suppressed by input filter	Fast mode	0		50	ns

I²C bus timing diagram



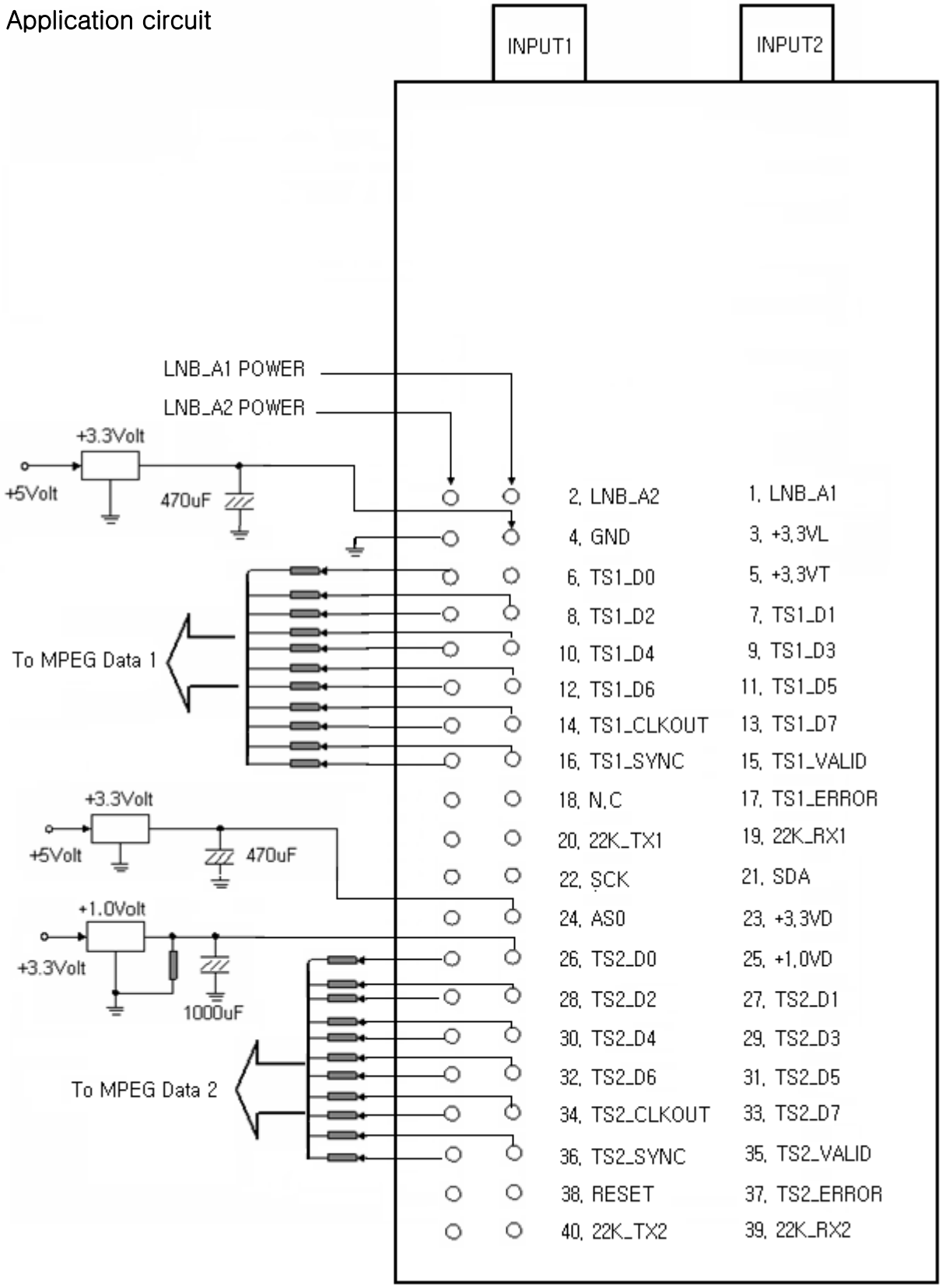
6. Block Diagrams



7. Pin Description

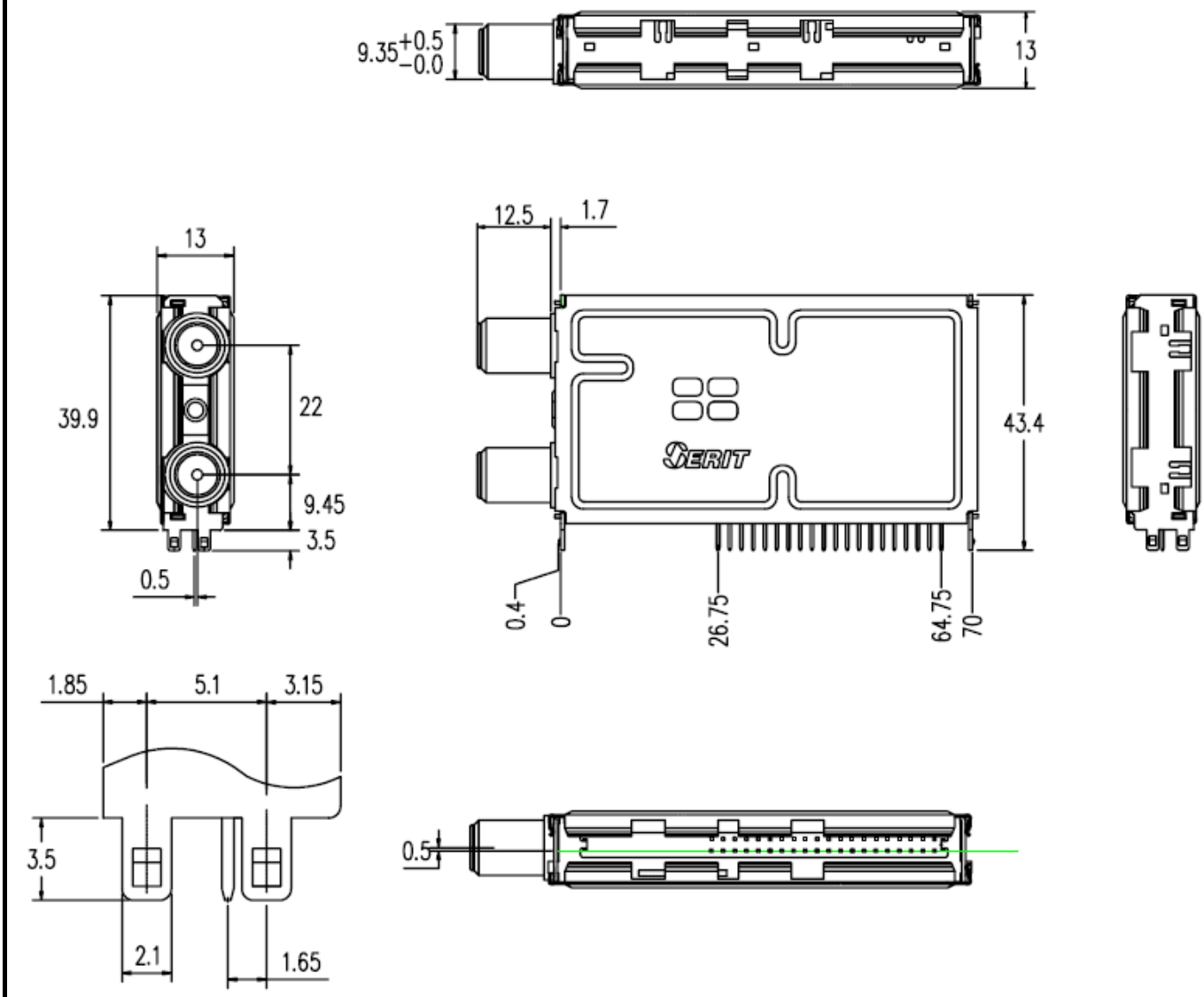
Pin No	Pin Name	Description
1	LNB_A1	LNB A1 voltage supply
2	LNB_A2	LNB A2 voltage supply
3	3.3VL	3.3Volt supply for LNA
4	GND	Ground
5	3.3VT	3.3Volt supply for ZIF IC
6~13	TS1_D0~TS1_D7	MPEG data1 interface data pins
14	TS1_CLKOUT	MPEG data1 interface clock pin
15	TS1_VALID	MPEG data1 interface control pin
16	TS1_SYNC	MPEG data1 interface control pin
17	TS1_ERROR	TS1 ERROR OUT
18	N.C	No Connection
19	22K_RX1	LNB 22KHz Receive Signal
20	22K_TX1	LNB 22KHz Transmit Signal
21	SDA	Serial programming interface data
22	SCL	Serial programming interface clock
23	3.3VD	3.3Volt supply for LINK IC
24	AS0	Address Select pin
25	1.0VD	1.0Volt supply for LINK IC
26~33	TS2_D0~TS2_D7	MPEG data2 interface data pins
34	TS2_CLKOUT	MPEG data2 interface clock pin
35	TS2_VALID	MPEG data2 interface control pin
36	TS2_SYNC	MPEG data2 interface control pin
37	TS2_ERROR	TS2 ERROR OUT
38	RESET	Chip reset
39	22K_RX2	LNB 22KHz Receive Signal
40	22K_TX2	LNB 22KHz Transmit Signal

8. Application circuit

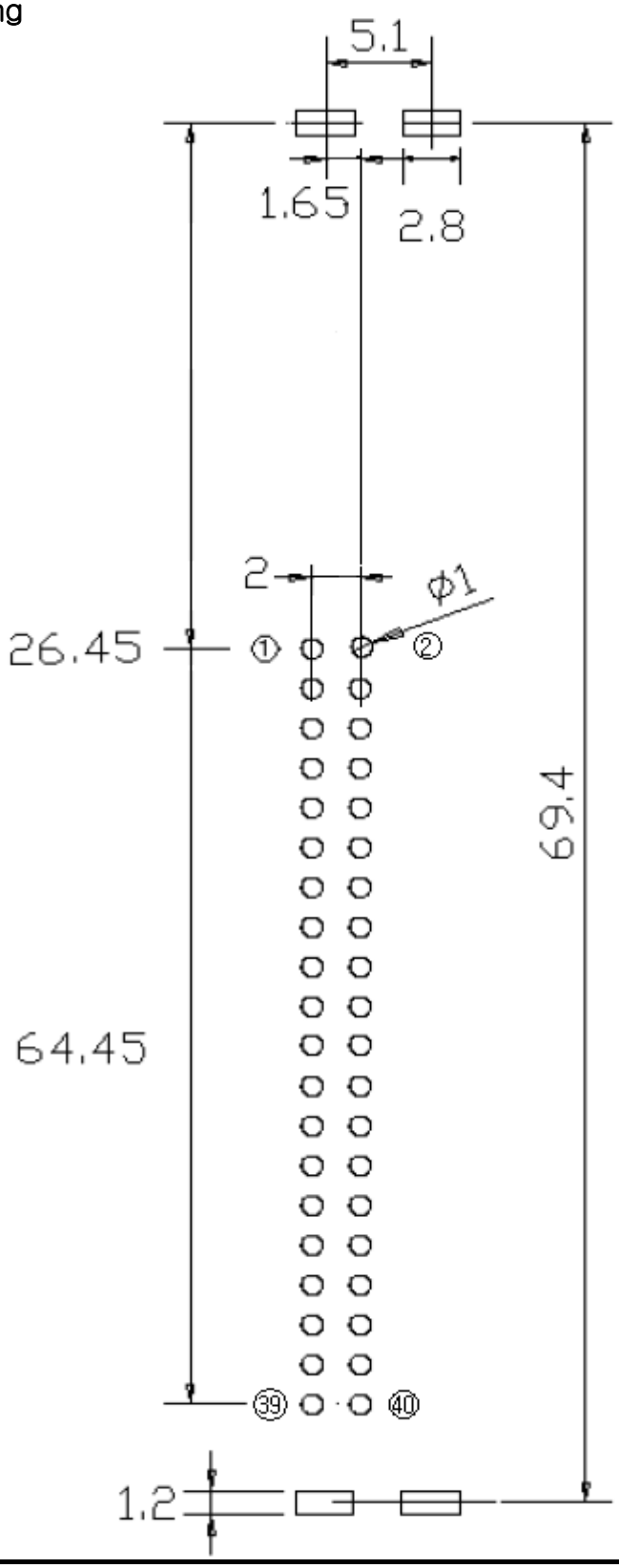


9. Outline Drawing

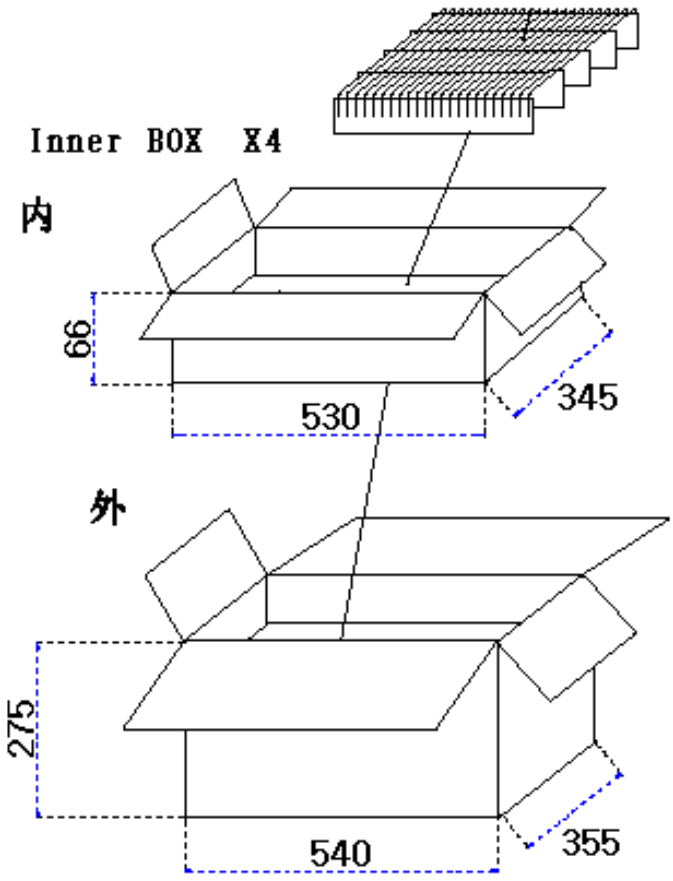
Vertical Chassis Type



10. Mounting Drawing



11. Packing Details



12. Electrostatic discharge

12.1 Test

Each front-end must be capable of normal performance after following tests:

ESD TEST

Test is performed with a voltage discharge From a 150 PF capacitor over a 330Ω series Resistor in the discharge path. There is a direct connect between the test probe head and the unit under test , using the test points and conditions detailed below:

- Test to pins 1 through 28

  4 successive ESD discharges of ±2KVDC between each pin and the front-end frame.

12.2 Handling

Anyone handling a front -end must wear a properly grounded anti -static Discharge bracelet to minimize ESD damage.

13. Heat load Test

- Measure the DUTs at room temperature
- Load the DUTs into chamber of the following conditions

  Temperature: 60℃

  Period: 160hrs

14. Cold Test

- Measure the DUTs at room temperature
- Load the DUTs into chamber of the following conditions

  Temperature: -20℃

  Period: 160hrs

15. Thermal shock

- Measure the DUTs at room temperature
- Load the DUTs into chamber of the following conditions

  Temperature: -40℃ for 60 min

  ↑ ↓

  110℃ for 60 min

  Period: 24 Cycle

16. Humidity load test

- Measure the DUTs at room temperature
- Load the DUTs into chamber of the following conditions

  Temperature: 40℃

  Humidity: 90%

  Period: 96hrs